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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,638	12/31/2001	Steven J. Tu	42390.P12490	9252

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EXAMINER	
TRIMMINGS, JOHN P	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,638	TU ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☒ Claim(s) *4,9 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 0201* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-30 are presented for examination.

Drawings

1. The drawings are objected to because FIG.3 330(1)...330(j) should instead be 350. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 4 and 9 are objected to because of the following informalities: the word "patter" should be "pattern". Appropriate correction is required.

3. Claim 12 is objected to because of the following informalities: the word "processor" should be "method". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 8, 20 and 29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the applicant does not teach in the specification, nor is there any reference within the drawings, to "a storage device to store a reset code module".

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 14 recites the limitation "each execution core" in line 2. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 21 recites the limitation "the first" (set of voltage nodes) in line 1. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 30 recites the limitation "the first set of voltage nodes" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 5-12, 22, and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bock et al., U.S. Patent No. 5155856.

As per Claim 1:

Bock et al. teaches an apparatus comprising: an execution core (FIG.3 1); a scan chain to transfer data to one or more nodes of the execution core (FIG.4 35); and a reset module (FIG.3) to provide a bit pattern to the scan chain (FIG.4 30), responsive to a reset signal (FIG.3 RRL and FIG.4 22x or 22y).

As per Claim 5:

Bock et al. further teaches the apparatus of claim 1, wherein the reset module further comprises: a clock mux (FIG.4 31) to provide a first (FIG.4 22a) or second clock signal to the scan chain, responsive to a reset signal (FIG.3 RRL or FIG.4 22x, 22y); and a pattern generator (FIG.4 30) to store the bit pattern and to provide the bit pattern

to the scan chain (FIG.4 D1), responsive to the reset signal (FIG.3 RRL and FIG.4 22x or 22y).

As per Claim 6:

Bock et al. further teaches the apparatus of claim 5, wherein the reset module further comprises a mode selector (FIG.3 RC) to assert a signal to the clock mux and the pattern generator, responsive to assertion of the reset signal (i.e. FIG.3 21 for μcode mode).

As per Claim 7:

Bock et al. further teaches the apparatus of claim 1, further comprising a reset tree (FIG.4 31, 33, 34) to propagate voltage states to selected nodes (FIG.4 F or I or S) of the execution core, responsive to the reset signal (FIG.3 RRL and FIG.4 22x or 22y).

As per Claim 8:

Bock et al. further teaches the apparatus of claim 1, further comprising a reset code module to step the execution core through a sequence of operations to establish states for additional nodes of the execution core (FIG.2 beginning at "RESET CONDITION?" decision box).

As per Claim 9:

Bock et al. further teaches a method for resetting a processor (FIG.1) comprising: detecting a reset event (FIG.2 Power on Reset for example); applying a bit pattern (FIG.4 D1) to a scan chain of the processor (FIG.4 S Decoder SRL), the bit pattern to drive specified states to one or more processor nodes (FIG.4 F or I or S) accessible through the scan chain.

As per Claim 10:

Bock et al. further teaches the method of claim 9, wherein applying the bit pattern comprises: applying a scan clock to a clock line of the scan chain (FIG.4 22a); and applying the bit pattern to a data line of the scan chain (FIG.4 D1).

As per Claim 11:

Bock et al. further teaches the method of claim 9, further comprising propagating the reset signal to selected nodes (FIG.4 S or I or F) of the processor through a reset tree (FIG.4 35).

As per Claim 12:

Bock et al. further teaches the method of claim 11, further comprising executing a reset code module to place additional nodes of the processor into specified states (FIG.2 decision box).

As per Claim 22:

Bock et al. teaches an apparatus comprising: an execution core (FIG.3 1) including a set of voltage nodes (FIG.4 35 S) coupled through data (FIG.4 D1) and clock lines (FIG.4 22, 23); a reset module (FIG.3) to drive a data signal (FIG.4 30) and a clock signal (FIG.4 22x, 22y) to the set of voltage nodes, responsive to occurrence of a reset event (FIG.3 POR), the data signal to place the voltage nodes of the set in specified logic states (in this case, 0's).

As per Claim 28:

Bock et al. further teaches the apparatus of claim 22, further comprising a reset tree to drive a second set of voltage nodes (FIG.4 35 I) of the apparatus to second logic states, responsive to occurrence of a reset event (FIG.3 IML).

As per Claim 29:

Bock et al. further teaches the apparatus of claim 28 further comprising a reset code module to be executed by the execution core to place a third set of voltage nodes in specified logic states, responsive to the reset event (FIG 2 decision box).

As per Claim 30:

Bock et al. further teaches the apparatus of claim 29, wherein the reset module establishes specified logic states for the first set of voltage nodes before the reset code module is executed (FIG.2 decision box comes after POR or IML reset).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-4 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bock et al., U.S. Patent No. 5155856, and in view of Milburn, U.S. Patent No. 5758058.

As per Claims 2 and 13:

Bock et al. further teaches the apparatus and method of claims 1 and 9, wherein the scan chain includes first scan chains corresponding to a first execution core, respectively (FIG.4 35). However, Bock et al. fails to teach wherein the execution core includes two execution cores to be operated in FRC mode. In an analogous art, Milburn does teach this feature of 2 processors operating in an FRC mode (column 1 lines 6-12). And in column 2 lines 16-45 cites the advantage of being able to thoroughly reset an FRC system in order to assure both processors are in lock-step. One with ordinary skill in the art at the time of the invention, motivated as suggested by Milburn, would find it obvious to include the improved microcode of Milburn to the reset procedure of Bock et al. in order to more thoroughly reset FRC processors.

As per Claims 3, 4 and 14:

Milburn further teaches the apparatus and method of claims 2 and 11, wherein the reset module provides an identical bit pattern to the first and second processors (column 9 lines 5-6), responsive to the reset signal (FIG.5 502). Not specifically specified by Milburn is input scan chains attached to the processors. However, in Bock et al., the main and the floating point processors (FIG3 1, 8) are arranged in a parallel manner, and are each loaded with the same input data (FIG.4 D1), thus parallel and simultaneous loading is further taught by Bock et al. And in view of the motivation above, the claims are rejected.

As per Claim 15:

Bock et al. fails to further teach the method of claim 9, comprising detecting an operating mode for the processor. The analogous art of Milburn however does teach

this feature in column 7 lines 24-38, and in view of the motivation previously stated, the claim is rejected.

10. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bock et al., U.S. Patent No. 5155856, in view of Milburn, U.S. Patent No. 5758058, and further in view of Colley et al., U.S. Patent No. 4325120. Bock et al. further teaches the method of claim 15, wherein the scan chain includes first scan chains corresponding to a first execution core, respectively (FIG.4 35), and a bit pattern is applied to the chain (FIG.4 D1). But Bock et al. and Milburn together fail to further teach the method of claim 15, wherein detecting the operating mode comprises determining if the operating mode is a high performance mode or a high reliability mode, and resetting the processor based on the mode. But Colley et al. does teach these features in an FRC/High Performance data processing system in the Abstract, and paragraphs 2057 and 2059. And Colley et al. in column 5 lines 33-39 boasts of the advantage of easily adding processors to the configuration to obtain higher performance of the system. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to apply the teachings of Colley et al., by adding processors to the system of Milburn and Bock et al. in order to increase performance.

11. Claims 17-21 and 23-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Colley et al., U.S. Patent No. 4325120, in view of Bock et al., U.S. Patent No. 5155856.

As per Claim 17:

Colley et al. teaches a system comprising: first and second execution cores to be operated in an FRC mode, responsive to a mode bit; an FRC checker to be activated in FRC mode to compare data from the first and second execution cores (paragraph 2096, section 10.4.4), but fails to teach a reset module to apply a bit pattern to scan chains of the execution cores, responsive to a reset event in the system. Bock et al., in an analogous art does teach the reset module (FIG.3), bit pattern (FIG.4 30, D1), scan chains (FIG.4 35), responsive to a reset event (FIG.3 RRL). And in column 1 lines 37-62 the advantage stated is that the invention offers selective reset of system hardware and states in response to the type of error or state of the system. And one with ordinary skill in the art at the time of the invention, motivated as above, would find it to be obvious to combine the selective capabilities of Bock et al. with the multiprocessor system of Colley et al. in order to more effectively handle such resets.

As per Claim 18:

Bock et al. further teaches the system of claim 17, wherein the reset module includes a pattern generator (FIG.4 30) to drive the bit pattern (FIG.4 D1) on data lines of the scan chains (FIG.4 35) of the execution cores responsive to a scan clock (FIG.4 22, 23). And in view of the motivation previously stated, the claim is rejected.

As per Claim 19:

Bock et al. further teaches the system of claim 18, further comprising a reset tree (FIG.4 F, I, S), the reset tree including electrical connections to a second set of nodes (FIG.4 33) to drive the second set of nodes to specified states responsive to the reset

event (FIG.4 22x, 22y). And in view of the motivation previously stated, the claim is rejected.

As per Claim 20:

Bock et al. further teaches the system of claim 18, further comprising a reset code module (FIG.2 decision box) to be executed by the execution cores to drive a third set of nodes (FIG.4 F and FIG.2 CHECK RESET F AREA) to specified states, responsive to the reset event (FIG.2 CHECK RESET). And in view of the motivation previously stated, the claim is rejected.

As per Claim 21:

Bock et al. further teaches the system of claim 20, wherein first, second and third sets of nodes are mutually exclusive (FIG.4 S, I, F). And in view of the motivation previously stated, the claim is rejected.

As per Claim 23:

Bock et al. further teaches the apparatus of claim 22, each execution core having a set of voltage nodes (FIG.4 35) coupled through clock (FIG.4 22, 23) and data lines (FIG.4 D1), but fails to teach wherein the execution core comprises first and second execution cores, the first and second execution cores to be operated in an FRC mode. But Colley et al. teaches this feature in the Abstract of the patent and paragraph 2057. And in view of the motivation previously stated for Colley et al., the claim is rejected.

As per Claim 24:

Bock et al. further teaches the apparatus of claim 23, wherein the data signal driven by the reset module (FIG.4 D1) is a bit pattern (0's in this case) that places the

set of voltage nodes of the execution cores in the specified logic states (FIG.4 35). And in view of the motivation previously stated, the claim is rejected.

As per Claim 25:

Bock et al. further teaches the apparatus of claim 24, wherein the reset module (FIG.3 RC) drives the set of voltage nodes of the first and second execution cores in parallel (FIG.3 1, 8). And in view of the motivation previously stated, the claim is rejected.

As per Claim 26:

Colley et al. further teaches the apparatus of claim 22, wherein the execution core comprises first and second execution cores, each having a set of voltage nodes, the first and second execution cores to be operated in an FRC mode, responsive to a mode bit being in a first state (see paragraph 2050 entitled MASTER). And in view of the motivation previously stated, the claim is rejected.

As per Claim 27:

Colley et al. further teaches the apparatus of claim 26, wherein the reset module is disabled and the execution cores are operated in a non-FRC mode, responsive to the mode bit being in a second state (see paragraphs 2057 and 2096). And in view of the motivation previously stated, the claim is rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-

0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Albert DeCady
Primary Examiner